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(54) LAMINATED SUBSTRATE BODY AND SEMICONDUCTOR DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To obtain a semiconductor device which is able to realize intended function in a short delivery time and has the high degree of integration.
SOLUTION: A laminated chip 4 is constituted by means of bonding pads 8a, 8b,... of a first chip 8 and pads 6a, 6b,... of a second chip 6. In the first chip 8, a field programmable gate array FPGA is formed. In the second chip 6, a central processing unit CPU is formed. An LSI 2 is used as a controller for controlling, e.g. an outer device. In this case, the FPGA functions as an interface circuit for linking the CPU with the outer device. By changing the FPGA program, the intended interface circuit corresponding to the outer device can be obtained. Furthermore through the use of

the laminated chip 4, this kind of controller the requirement for space saving of which is large, can be made compact.

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CLAIMS

[Claim(s)]
[Claim 1] The 1st programmable function part which acquires a desired function by carrying out on/off of two or more circuit elements of both prepared beforehand using a programmable switching means, The 1st substrate which has the 1st input/output terminal corresponding to the 1st function part, So that it may have the 2nd substrate which has the 2nd function part equipped with the function relevant to the 1st function part, and the 2nd input/output terminal corresponding to the 2nd function part and the 1st input/output terminal and 2nd input/output terminal may be connected electrically The laminating radical board characterized by carrying out the laminating of the 1st substrate and 2nd substrate.
[Claim 2] What is characterized by equipping said 2nd function part with the function

which controls an external instrument in the laminating radical board of claim 1, and equipping said 1st function part with the interface function which connects the 2nd function part and external instrument concerned.

[Claim 3] What is characterized by equipping said 2nd function part with the function to memorize information, in the laminating radical board of claim 1, and having the function in which said 1st function part performs processing relevant to the information memorized by the 2nd function part.

[Claim 4] What is characterized by equipping said 2nd function part with the function to perform analog processing, in the laminating radical board of claim 1, and having the function in which said 1st function part performs digital processing relevant to the analog processing performed by the 2nd function part.

[Claim 5] What is characterized by equipping said 2nd function part with the function which controls said 1st function part in the laminating radical board of claim 1.

[Claim 6] What is characterized by constituting so that power may be supplied to said 2nd substrate through the 1st substrate in the laminating radical board of either claim 1 thru/or claim 5 while supplying the power from a power source to said 1st substrate.

[Claim 7] The 1st function part equipped with the function to memorize information, and the 1st input/output terminal corresponding to the 1st function part, The 1st substrate which ****, and the 2nd function part equipped with the function which controls the 1st function part, The laminating radical board characterized by carrying out the laminating of the 1st substrate and 2nd substrate so that it may have the 2nd substrate which has the 2nd input/output terminal corresponding to the 2nd function part and the 1st input/output terminal and 2nd input/output terminal may be connected electrically.

[Claim 8] What is characterized by constituting so that said the 1st substrate and 2nd substrate may be equipped with both high-voltage Rhine and the electrical potential difference of high-voltage Rhine of the 1st substrate and the electrical potential difference of high-voltage Rhine of the 2nd substrate may become the same substantially in the laminating radical board of either claim 1 thru/or claim 7.

[Claim 9] What is characterized by constituting so that two or more sets of pairs of the 1st input/output terminal for connecting electrically high-voltage Rhine of said 1st substrate and high-voltage Rhine of the 2nd substrate and the 2nd input/output terminal may be prepared in the laminating radical board of claim 8.

[Claim 10] In the laminating radical board of either claim 1 thru/or claim 9 to either said 1st substrate or the 2nd substrate What is characterized by constituting so that either said 1st input/output terminal belonging to the substrate with which the terminal for the exteriors which performs the input or output to the exterior of the laminating radical board concerned was prepared, and said terminal for the exteriors was prepared or the 2nd input/output terminal and the terminal for the exteriors concerned may be connected electrically.

[Claim 11] The semiconductor device characterized by having the laminating radical board of either claim 1 thru/or claim 10.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] Especially this invention relates to the semiconductor device equipped with the laminating radical board and laminating radical board which carried out the laminating of the substrate about a substrate and a semiconductor device.

[0002]

[Description of the Prior Art] PLD (Programmable Logic Device) is known as LSI in which a user can write a logical function with a hand. There are many classes of PLD(s) until it results in large-scale FPGA (Field Programmable Gate Array) from small-scale PLA (Programmable Logic Array) which makes basic structure an AND flat surface and OR flat surface.

[0003] Each of these constitutes mutual [, such as a logical circuit,] so that it can connect through a programmable switch, while arranging many logical circuits etc. on a chip beforehand. Therefore, a user can realize a desired logical function by carrying out on/off of the switch of these many according to a predetermined pattern. That is, LSI which has a desired logical function is realizable at short time for delivery by using PLD.

[0004] For this reason, for example, PLD is used as an interface circuitry of the microcomputer system which controls a device. In a microcomputer system, although the interface circuitry of the dedication corresponding to the device used as a controlled system is needed, by using PLD, it is short time for delivery and the interface circuitry of the request corresponding to various devices can be realized.

[0005]

[Problem(s) to be Solved by the Invention] However, there were the following troubles in the above conventional PLD(s). Since the conventional PLD is constituted by one independent package, for example, when it uses for an above-mentioned microcomputer system, one package is needed only by the interface circuitry. The degree of integration of a microcomputer system cannot be raised in this.

[0006] This invention solves such a trouble and it aims at being able to realize a desired function at short time for delivery, and offering a semiconductor device with a high degree of integration.

[0007]

[Means for Solving the Problem] The 1st programmable function part which acquires a desired function when the laminating radical board of claim 1 carries out on/off of two or more circuit elements of both prepared beforehand using a programmable switching means, The 1st substrate which has the 1st input/output terminal corresponding to the 1st function part, It is characterized by carrying out the laminating of the 1st substrate and 2nd substrate so that it may have the 2nd substrate which has the 2nd function part equipped with the function relevant to the 1st function part, and the 2nd input/output terminal corresponding to the 2nd function part and the 1st input/output terminal and 2nd input/output terminal may be connected electrically.

[0008] The laminating radical board of claim 2 is characterized by equipping said 2nd function part with the function which controls an external instrument, and equipping said 1st function part with the interface function which connects the 2nd function part and external instrument concerned in the laminating radical board of claim 1.

[0009] The laminating radical board of claim 3 is characterized by equipping said 2nd function part with the function to memorize information, and having the function in which said 1st function part performs processing relevant to the information memorized by the 2nd function part in the laminating radical board of claim 1.

[0010] The laminating radical board of claim 4 is characterized by equipping said 2nd function part with the function to perform analog processing, and having the function in which said 1st function part performs digital processing relevant to the analog processing performed by the 2nd function part in the laminating radical board of claim 1.

[0011] The laminating radical board of claim 5 is characterized by equipping said 2nd function part with the function which controls said 1st function part in the laminating radical board of claim 1.

[0012] In the laminating radical board of either claim 1 thru/or claim 5, the laminating radical board of claim 6 is characterized by constituting so that power may be supplied to said 2nd substrate through the 1st substrate while it supplies the power from a power source to said 1st substrate.

[0013] The 1st function part which the laminating radical board of claim 7 equipped with the function to memorize information, The 1st substrate which has the 1st input/output terminal corresponding to the 1st function part, It is characterized by carrying out the laminating of the 1st substrate and 2nd substrate so that it may have the 2nd substrate which has the 2nd function part equipped with the function which controls the 1st function part, and the 2nd input/output terminal corresponding to the 2nd function part and the 1st input/output terminal and 2nd input/output terminal may be connected electrically.

[0014] In the laminating radical board of either claim 1 thru/or claim 7, said the 1st substrate and 2nd substrate are equipped with high-voltage Rhine, and both the

laminating radical boards of claim 8 are characterized by constituting so that the electrical potential difference of high-voltage Rhine of the 1st substrate and the electrical potential difference of high-voltage Rhine of the 2nd substrate may become the same substantially.

[0015] The laminating radical board of claim 9 is characterized by constituting so that two or more sets of pairs of the 1st input/output terminal for connecting electrically high-voltage Rhine of said 1st substrate and high-voltage Rhine of the 2nd substrate and the 2nd input/output terminal may be prepared in the laminating radical board of claim 8.

[0016] The laminating radical board of claim 10 is set to the laminating radical board of either claim 1 thru/or claim 9. Either said 1st input/output terminal belonging to the substrate with which the terminal for the exteriors which performs the input or output to the exterior of the laminating radical board concerned was prepared in either said 1st substrate or the 2nd substrate, and said terminal for the exteriors was prepared in it, or the 2nd input/output terminal. It is characterized by constituting so that the terminal for the exteriors concerned may be connected electrically.

[0017] The semiconductor device of claim 11 is characterized by having the laminating radical board of either claim 1 thru/or claim 10.

[0018] In addition, the "circuit element" in each above-mentioned claim is a concept which says the element which constitutes a circuit, for example, includes all components and circuits, such as a logical element, a delay element, a storage element, an arithmetic circuit, and wiring. With an operation gestalt, data input Rhine L11 of drawing 3 , the ... and AND input line L21, ..., etc. correspond to this.

[0019] An "input/output terminal" is a concept containing the input-only terminal which says the terminal which performs a certain input or output, for example, receives supply of a signal or power, the output-only terminal for supplying, an I/O combination terminal, etc. With an operation gestalt, the pads 8a and 8b of drawing 1 , ... and Pads 6a and 6b, and ... correspond to this.

[0020]

[Function and Effect of the Invention] The laminating radical board of claim 1, and the semiconductor device of claim 11 The 1st substrate which has the 1st programmable function part and 1st programmable input/output terminal, It is characterized by carrying out the laminating of the 1st substrate and 2nd substrate so that it may have the 2nd substrate which has the 2nd function part equipped with the function relevant to the 1st function part, and the 2nd input/output terminal and the 1st input/output terminal and 2nd input/output terminal may be connected electrically.

[0021] Therefore, the 2nd function part and external instrument can be made to be able to respond, and the function of the 1st function part can be changed flexibly. For this reason, the function of the 1st function part can be realized, without building the new dedication IC. Moreover, the semiconductor device which has a small projected

area equipped with both the function of the 1st function part and the function of the 2nd function part is realizable by carrying out the laminating of the 1st substrate and 2nd substrate. Furthermore, the complicated system which constituted many the 1st substrate and 2nd substrate from carrying out a laminating using many ICs is realizable with one semiconductor device. For this reason, it becomes possible to be low cost and to realize such a system in a compact.

[0022] That is, a desired function can be realized at short time for delivery, and a cheap semiconductor device with a high degree of integration can be obtained.

[0023] The laminating radical board of claim 2 is characterized by having the function in which the 2nd function part controls an external instrument, and equipping the 1st function part with the interface function which connects the 2nd function part and external instrument concerned.

[0024] When it follows, for example, a laminating radical board is used for the control unit of an external instrument, an external instrument can be made to be able to respond and an interface function can be changed flexibly. Moreover, a space-saving demand can use a large control unit as a compact by using a laminating radical board.

[0025] The laminating radical board of claim 3 is characterized by having the function in which the 2nd function part memorizes information, and having the function in which the 1st function part performs processing relevant to the information memorized by the 2nd function part.

[0026] When it follows, for example, a laminating radical board is used for DSP (digital signal processor), while using the 2nd function part as RAM (random access memory), it can be made to be able to respond to the contents of signal processing, and the function of the 1st function part can be changed flexibly. Moreover, compact DSP can be obtained by using a laminating radical board.

[0027] The laminating radical board of claim 4 is characterized by having the function in which the 2nd function part performs analog processing, and having the function in which the 1st function part performs digital processing relevant to the analog processing performed by the 2nd function part.

[0028] When it follows, for example, a laminating radical board is used for the frequency synthesizer using a PLL (phase-locked loop) circuit, while using the 2nd function part as VCO (armature-voltage control dispatch circuit), the 1st function part can be used as a frequency divider which carries out dividing of the output of VCO. In this case, it can be made to be able to respond to the frequency which should be outputted and a frequency divider can be changed flexibly. Moreover, a compact frequency synthesizer can be obtained by using a laminating radical board.

[0029] The laminating radical board of claim 5 is characterized by equipping the 2nd function part with the function which controls said 1st function part.

[0030] It follows, for example, when the 2nd function part is used as write-in equipment for programming the 1st function part, PLD which does not need external

write-in equipment can be realized.

[0031] The laminating radical board of claim 6 is characterized by constituting so that power may be supplied to the 2nd substrate through the 1st substrate while it supplies the power from a power source to the 1st substrate.

[0032] Therefore, to the 1st substrate which the writing and elimination of the program over the 1st function part take the high voltage, high-voltage power is supplied with low-battery power from a power source, and it becomes possible at it to supply only low-battery power through the 1st substrate at the 2nd substrate which does not require the high voltage. For this reason, it is enough if only the 1st substrate is made into a high proof-pressure specification. That is, since the 2nd substrate can be made into a low proof-pressure specification, the degree of integration of the circuit element which constitutes the 2nd substrate can be raised.

[0033] The 1st substrate which has the 1st function part which the laminating radical board of claim 7 equipped with the function to memorize information, and the 1st input/output terminal, It has the 2nd substrate which has the 2nd function part equipped with the function which controls the 1st function part, and the 2nd input/output terminal, and is characterized by carrying out the laminating of the 1st substrate and 2nd substrate so that the 1st input/output terminal and 2nd input/output terminal may be connected electrically.

[0034] When it follows, for example, the 2nd function part is used as informational write-in equipment to the 1st function part, the information storage device which does not need external write-in equipment can be realized. Moreover, the information storage device which has a small projected area equipped with both the function to memorize information, and the function which writes in information is realizable by carrying out the laminating of the 1st substrate and 2nd substrate.

[0035] The 1st substrate and 2nd substrate are equipped with high-voltage Rhine, and both the laminating radical boards of claim 8 are characterized by constituting so that the electrical potential difference of high-voltage Rhine of the 1st substrate and the electrical potential difference of high-voltage Rhine of the 2nd substrate may become the same substantially.

[0036] Therefore, high-voltage Rhine of the 1st substrate and high-voltage Rhine of the 2nd substrate can be shared with both substrates by connecting the 1st input/output terminal and 2nd input/output terminal electrically. For this reason, a tooth space required for wiring for high voltages etc. can be saved.

[0037] The laminating radical board of claim 9 is characterized by constituting so that two or more sets of pairs of the 1st input/output terminal for connecting electrically high-voltage Rhine of the 1st substrate and high-voltage Rhine of the 2nd substrate and the 2nd input/output terminal may be prepared.

[0038] Therefore, even if it is the case that the connection resistance at the time of connecting the 1st input/output terminal and 2nd input/output terminal is strong, this

connection resistance can be decreased by establishing two or more connection places.

[0039] The laminating radical board of claim 10 is characterized by constituting so that either the 1st input/output terminal belonging to the substrate with which the terminal for the exteriors was prepared in either the 1st substrate or the 2nd substrate, and the terminal for the exteriors was prepared or the 2nd input/output terminal and the terminal for the exteriors concerned may be connected electrically.

[0040] When it follows, for example, the terminal for the exteriors is prepared in the 1st substrate, the terminal for the exteriors and the 2nd input/output terminal of the 2nd substrate concerned can be electrically connected through the 1st input/output terminal of the 1st substrate. For this reason, it becomes possible between the 2nd substrate with which the terminal for the exteriors is not prepared, and the terminal for the exteriors to perform transfer of power or a signal directly.

[0041]

[Embodiment of the Invention] The cross-section configuration of LSI (large scale integration)2 which is a semiconductor device by 1 operation gestalt of this invention is shown in drawing 1 . LSI2 has the configuration which laid the laminating chip 4 which is a laminating radical board, and was fixed after the package 12. The laminating chip 4 is a chip which carried out the laminating of the 2nd chip 6 which is the 1st chip 8 and the 2nd substrate which are the 1st substrate, and was unified.

[0042] The decomposition perspective view of the laminating chip 4 is shown in drawing 2 . The 1st chip 8 and the 2nd chip 6 are IC chips constituted by each with the semi-conductor. In this operation gestalt, FPGA (field programmable gate array) is formed in the 1st chip 8 as the 1st programmable function part, and CPU (central-process unit) is formed in the 2nd chip 6 as the 2nd function part.

[0043] The 1st chip 8 equips the top face with two or more pads 8a and 8b and ... which are the 1st input/output terminal. In this operation gestalt, it is a pad for performing I/O of as opposed to FPGA in Pads 8a and 8b and ... Moreover, near the periphery of the top face of the 1st chip 8, two or more pads 10 (terminal for the exteriors) for performing the I/O to the exterior are formed.

[0044] The 2nd chip 6 equips the inferior surface of tongue with two or more pads 6a and 6b and ... which are the 2nd input/output terminal. In this operation gestalt, it is a pad for performing I/O of as opposed to CPU in Pads 6a and 6b and ...

[0045] It is prepared in the location where each pads 8a and 8b, ... and Pads 6a and 6b, and ... counter mutually. Pads 8a and 8b, ... and Pads 6a and 6b, and ... are joined with the bump technique using an eutectic by forming one side with the pads 8a and 8b prepared in the location which opposes mutually, ... and Pads 6a and 6b, and ... withgold (Au), and forming another side with tin (Su).

[0046] Thus, the formed laminating chip 4 is laid and fixed after a package 12, as shown in drawing 1 . The pad 14 prepared in the package 12 and the pad 10 prepared

in the 1st chip 8 are connected by the bonding wire 16. In addition, the closure of the laminating chip 4 and the bonding wire 16 is carried out by the closure member (not shown) which used the epoxy resin etc.

[0047] In this operation gestalt, LSI2 is used as a controller which controls an external instrument. That is, an external instrument is controlled using CPU (not shown) formed in the 2nd chip 6. An external instrument is electrically connected to the pad 14 prepared in the package 12. FPGA formed in the 1st chip 8 functions as an interface circuitry which connects CPU and an external instrument.

[0048] Therefore, the interface circuitry of the request corresponding to an external instrument can be obtained by changing the program of FPGA. For this reason, a desired interface circuitry can be realized, without building IC with a new dedicated-interface circuit. That is, it is not necessary to develop the new dedication IC or to prepare the production process for Dedication IC separately.

[0049] Moreover, a space-saving demand can form this large kind of controller in a compact by using the laminating chip 4. In addition, in this operation gestalt, as a ROM (read only memory) chip (not shown), the program for controlling an external instrument is arranged to the exterior of LSI2, and is sent to CPU through the pad 14 prepared in the package 12.

[0050] Moreover, the power source (not shown) is prepared in the exterior of LSI2, from the power source concerned, power is supplied to the 1st chip 8 through a pad 14, and power is further supplied to the 2nd chip 6 through the 1st chip 8.

[0051] Therefore, to the 1st chip 8 which the writing and elimination of the program over FPGA take the high voltage, high-voltage power is supplied with low-battery power from a power source, and it becomes possible for it to supply only low-battery power through the 1st chip 8 at the 2nd chip 6 which carried CPU which does not require the high voltage. For this reason, it is enough if only the 1st chip 8 is made into a high proof-pressure specification. That is, since the 2nd chip 6 can be made into a low proof-pressure specification, the degree of integration of the 2nd chip 6 which carried CPU can be raised.

[0052] An example of the circuitry of the logic array 20 which constitutes FPGA formed in drawing 3 at the 1st chip 8 is shown typically. FPGA is PLD of a comparatively complicated configuration and the logic array 20 of FPGA is equipped with the AND flat-surface section 22 and OR flat-surface section 24. In addition, drawing 3 is drawing having extracted and shown a part of circuitry of logic array 20 for explanation, and the actual logic array 20 has a more complicated configuration.

[0053] The AND flat-surface section 22 is equipped with four data input Rhine L11, L12, L13, and L14 and four AND input lines L21, L22, L23, and L24 which are circuit elements, and the four AND gates AND1, AND2, AND3, and AND4 in the example of drawing 3 .

[0054] The switches SW11-SW44 which are programmable switching means are

formed in 16 intersections of the data input Rhine L11-L14 and the AND input lines L21-L24 of the AND flat-surface section 22.

[0055] OR flat-surface section 24 is equipped with four AND output Rhine L31, L32, L33, and L34 and three OR input lines L41, L42, and L43 which are circuit elements, the three OR gates OR1, OR2, and OR3, and three OR output Rhine L51, L52, and L53.

[0056] The switches SW51-SW83 which are programmable switching means are formed in 12 intersections of the AND output Rhine L31-L34 and the OR input lines L41-L43 of OR flat-surface section 24 like the AND flat-surface section 22.

[0057] In addition, although it indicated for convenience that drawing 3 used [of explanation] the four AND gates AND1, AND2, AND3, and AND4 and the three OR gates OR1, OR2, and OR3, in an actual circuit, it changed to these gates and the equivalent circuit is logically realized with drawing 3 using seven NAND gates.

[0058] The example of a programmable switching means (for example, switch SW11) is shown in drawing 4 A, drawing 4 B, and drawing 4 C. As a switch SW11, the fuse shown in drawing 4 A can be used. In this case, what is necessary is just to burn off this fuse, in order to separate data input Rhine L11 and the AND input line L21.

[0059] Contrary to the case of a fuse, it insulates beforehand and the antifuse (not shown) constituted so that it might be made to flow through data input Rhine L11 and the AND input line L21 can also be used as a switch SW11 by destroying an insulation. Moreover, the flash memory and EEPROM (Erectrically Erasable and Programmable Read Only Memory) which are shown in drawing 4 B can also be used as a switch SW11. It becomes rewritable [a logical function] by using EEPROM.

[0060] Moreover, in order to make a logical function rewrite on real time, SRAM (Static Random Access Memory) shown in drawing 4 C can also be used as a switch SW11.

[0061] Furthermore, the memory using the ferroelectric as a switch SW11 can also be used. By using the memory using a ferroelectric, the switch SW11 rewritable at high speed nonvolatile is realizable.

[0062] An example of the circuitry of the switch SW11 which used the memory which used the ferroelectric for drawing 5 is shown. The switch SW11 is equipped with the ferroelectric transistor 30 in this example.

[0063] Although the ferroelectric layer FE is polarized if a predetermined electrical potential difference is impressed between gate terminal G and data input Rhine L11, the direction of polarization of the ferroelectric layer FE changes with sense of the electrical potential difference to impress. When the directions of polarization of the ferroelectric layer FE differ, the values of the drain current over the same gate voltage differ. Using this property, it constitutes so that the closed state and open condition of a switch SW11 may be made.

[0064] The relation between the sense of the electrical potential difference impressed between gate terminal G and data input Rhine L11 and the direction of polarization of

the ferroelectric layer FE brings the same relation at least to the bottom of the same condition, although it was not necessarily fixed in order to be influenced of other elements.

[0065] If the electrical potential difference of the sense from which it follows, for example, gate terminal G becomes forward to data input Rhine L11 is impressed If it polarizes to predetermined gate voltage in the direction in which the drain current more than a threshold flows and the electrical potential difference of the reverse sense is impressed, supposing it polarizes to predetermined gate voltage in the direction in which only the drain current of a value smaller than a threshold flows The former is the closed state of a switch SW11, and the latter is in the open condition of a switch SW11.

[0066] Thus, the on/off data of a switch SW11 can be rewritten by changing the sense of the electrical potential difference impressed between gate terminal G and data input Rhine L11.

[0067] In addition, although it constituted so that the direction of polarization of the ferroelectric layer FE might be changed by changing the sense of the electrical potential difference impressed between gate terminal G and data input Rhine L11 in the example of drawing 5 By connecting an electrode terminal to gate terminal G of the ferroelectric layer FE, and the edge of the opposite side, setting this to memory gate terminal MG, and changing the sense of the electrical potential difference impressed between gate terminal G and memory gate terminal MG, it can also constitute so that the direction of polarization of the ferroelectric layer FE may be changed.

[0068] Moreover, the memory (not shown) equipped with the ferro-electric capacitor in addition to the memory equipped with the ferroelectric transistor 30 shown in drawing 5 as memory using the ferroelectric for using it for a switch SW11 can also be used.

[0069] In addition, in an above-mentioned operation gestalt, although the case where LSI2 was used as a controller which controls an external instrument was explained to the example, this invention is not limited to this. For example, this invention can be applied also when used as FPGA with general-purpose LSI2.

[0070] In this case, FPGA is formed in the 1st chip 8 as the 1st function part like the above-mentioned operation gestalt. On the other hand, the write-in circuit which performs the writing and elimination of the program to FPGA is formed in the 2nd chip 6 as the 2nd function part. If it does in this way, FPGA which does not need external write-in equipment is realizable.

[0071] Moreover, this invention can be applied also when using LSI2 as a DSP (digital signal processor). In order to use LSI2 as a DSP, RAM (random access memory) is formed in the 2nd chip 6 as the 2nd function part.

[0072] On the other hand, for the 1st chip 8, like the above-mentioned operation

gestalt, although FPGA is formed as the 1st function part, it programs so that FPGA functions as the signal-processing section in this case.

[0073] Thus, if it sets up, after FPGA performs predetermined processing to the signal given from RAM formed in the 2nd chip 6, it can be outputted to the LSI2 exterior, or after performing predetermined processing to the signal given from the LSI2 outside, it can be accumulated in RAM formed in the 2nd chip 6.

[0074] By changing the program of FPGA, the contents of signal processing can be changed easily. Moreover, compact DSP is realizable by using the laminating chip 4.

[0075] Moreover, for example, while forming FPGA in the 1st chip 8, it can also constitute so that a flash memory may be formed in the 2nd chip 6. In this case, FPGA of the 1st chip 8 and the flash memory of the 2nd chip 6 may need high-voltage Rhine for writing and elimination. In such a case, it is convenient, if it sets up so that the electrical potential difference which the writing and elimination of FPGA take, and the electrical potential difference which the writing and elimination of a flash memory take may become the same.

[0076] If the electrical potential difference is set up in this way, high-voltage Rhine of 1st chip 8 and 2nd chip 6 both sides can be shared between the chips of the both sides concerned through Pads 8a and 8b, ..., 6a and 6b, or ... For this reason, a tooth space required for wiring for high voltages etc. can be saved.

[0077] If two or more sets of pads for furthermore connecting the high-voltage Rhine concerned in this case are formed, connection resistance can be made small and it is convenient. Especially the thing for which a node is formed in juxtaposition in this way, and connection resistance is made small since there is an inclination for connection resistance to become large in using an above-mentioned bump technique and the above-mentioned anisotropy conductor mentioned later is desirable as a connection method of Pads 8a and 8b, ..., 6a and 6b, and ...

[0078] Moreover, for example, LSI2 can be used as a frequency synthesizer using a PLL (phase-locked loop) circuit. In this case, VCO (armature-voltage control dispatch circuit) which is an analog circuit is formed in the 2nd chip 6 as the 2nd function part.

[0079] a circuit which is again fed back to VCO on the other hand after FPGA carries out dividing of the output of VCO in this case although FPGA is formed in the 1st chip 8 as the 1st function part like the above-mentioned operation gestalt -- ** -- it carries out and programs to function.

[0080] Thus, if it sets up, LSI2 can be used as a frequency synthesizer using a PLL circuit. In this case, the frequency which should be outputted can be easily changed by changing the program of FPGA. Moreover, a compact frequency synthesizer can be obtained by using the laminating chip 4.

[0081] In addition, the pad with which transfer of an analog signal is needed for it in this way when it carries an analog circuit in the 2nd chip 6 as the 2nd function part is good to use a buffer as the pad not intervening.

[0082] Moreover, a pad 10 and pad 6a of the 2nd chip 6 are electrically connectable through pad 8a what (through pad) for example, either of the pads 10 prepared in the 1st chip 8 in this case and pad 8a are made into switch-on for. For this reason, even if it is the case where the terminal for the exteriors cannot be directly prepared in the 2nd chip 6, the pad 10 prepared in the 1st chip 8 can be used as an input/output terminal of an analog signal, for example, or it can use as a power supply terminal only for [a pad 10] analog circuits, and is convenient.

[0083] In each above-mentioned operation gestalt, although the case where FPGA was formed in the 1st chip 8 as the 1st function part was explained to the example, this invention is not limited to this. For example, it can constitute so that a memory apparatus may be formed in the 1st chip 8 as the 1st function part. In this case, it is good for the 2nd chip 6 to form the write-in circuit which performs the writing and elimination of the data to this memory apparatus as the 2nd function part.

[0084] Thus, if constituted, the information storage device which does not need external write-in equipment is realizable. Moreover, the information storage device which has a small projected area equipped with both the function to memorize information, and the function which writes in information is realizable by carrying out the laminating of the 1st chip 8 and the 2nd chip 6.

[0085] In addition, in each above-mentioned operation gestalt, although the case where a bump technique was used was explained to the example as an approach of connecting electrically Pads 8a and 8b, ... and Pads 6a and 6b, and ... as shown in drawing 1 , this invention is not limited to this. For example, Pads 8a and 8b, ... and Pads 6a and 6b, and ... are also electrically connectable using a pewter technique.

[0086] Moreover, as shown in drawing 6 , Pads 6a and 6b and ... are also electrically connectable in Pads 8a and 8b and ... using the anisotropy conductor 18. The anisotropy conductor 10 is a conductor which has conductivity only in an one direction, and has the adhesive property. As an anisotropy conductor, ANISORUMU (Hitachi Chemical) which is thermosetting adhesives can be used.

[0087] By using such an anisotropy conductor 18, the 1st chip 8 and the 2nd chip 6 can be pasted up firmly. The pads 8a and 8b prepared in the location which counters mutually, ... and Pads 6a and 6b, and ... are electrically connected by pasting up firmly the 1st chip 8 and the 2nd chip 6 using the anisotropy conductor 18.

[0088] Moreover, in each above-mentioned operation gestalt, although it constituted so that the pad 10 of the laminating chip 4 and the pad 14 prepared in the package 12 might be connected using a bonding wire 16 while fixing the laminating chip 4 to the package 12 as shown in drawing 1 , this invention is not limited to such a configuration.

[0089] For example, as shown in drawing 7 , the laminating chip 4 can also be directly mounted in a film-like synthetic-resin substrate. Thus, the substrate which mounted the laminating chip 4 is called tab (tab:tape automated bonding) 26. The printed circuit (not shown) is given to the tab 26 and the pad section (not shown) of a printed circuit

and the pad 10 of the laminating chip 4 are joined. In addition, the closure of the laminating chip 4 is carried out like the case of each above-mentioned operation gestalt by the closure member (not shown) which used the epoxy resin etc.

[0090] Moreover, as shown in drawing 8 , when it is possible to form a pad 10 in the inferior surface of tongue (namely, Pads 8a and 8b, the field of the opposite side of the field in which ... was prepared) of the 1st chip 8, the laminating chip 4 can also be mounted so that it may accumulate on the top face of a tab 26.

[0091] In addition, in each above-mentioned operation gestalt, although it constituted so that power might be supplied to the 1st chip 8 and power might be further supplied to the 2nd chip 6 through the 1st chip 8, this invention is not limited to this. For example, it can also constitute so that power may be supplied to the 2nd chip 6 and power may be further supplied to the 1st chip 8 through the 2nd chip 6. Moreover, arrangement relation between the 1st chip 8 and the 2nd chip 6 can also be made into vertical reverse.

[0092] Moreover, in each above-mentioned operation gestalt, although the laminating chip 4 repeated two chips was explained to the example, this invention is applicable also to the laminating chip repeated three or more chips.

[0093] Drawing 9 is a drawing in which the laminating chip 36 which has the configuration which has arranged the 2nd chip 32 and the 3rd chip 34 side by side after the 1st chip 8 horizontally is shown. The laminating chip 36 is being laid and fixed to the package 12.

[0094] For example, if ROM is formed in the 3rd chip 34 while programming to form FPGA in the 1st chip 8 and to commit an interface circuitry and forming CPU in the 2nd chip 32, the controller for controlling an external instrument is realizable with one laminating chip 36. In addition, the 1st chip 8 corresponds to the 1st substrate in this case, and the 2nd chip 32 and the 3rd chip 34 correspond to the 2nd substrate.

[0095] Drawing 11 is the decomposition perspective view showing the laminating chip 52 which has the configuration which has arranged much chips (it corresponds to the 2nd substrate) 50a, 50b, ..., 50g side by side horizontally after the 1st chip 8 (it corresponds to the 1st substrate).

[0096] For example, while forming each function part 62 which constitutes the compact disc system 60 as shown in drawing 12 , for example, an RF amplifier, DSP64, DF-DAC66, the CD-G decoder 68, the RGB encoder 70, and CD driver 72 grade as chips 50a, 50b, ..., 50g of drawing 11 , respectively, it can form in the 1st chip 8 by setting the system-control microcomputer 74, connection during each chip (not shown), etc. to FPGA.

[0097] In addition, conventionally, the compact disc system 60 shown in drawing 12 formed each function part of RF amplifier 62, DSP64, DF-DAC66, the CD-G decoder 68, the RGB encoder 70, the CD driver 72, and system-control microcomputer 74 grade as a different IC, respectively, and it constituted it so that these might be

carried in one board. Therefore, compactability was missing and the manufacturing cost was also high.

[0098] If constituted like drawing 11 , a complicated system like the compact disc system 60 realized by carrying two or more ICs in one board conventionally is realizable with one laminating chip 52, i.e., one IC. For this reason, a complicated system is realizable by the compact and low cost.

[0099] Drawing 10 is a drawing in which the laminating chip 44 which has the configuration which carried the 3rd chip 42 and was fixed after the 2nd chip 40 is shown while it carries the 2nd chip 40 and is fixed after the 1st chip 8. The laminating chip 44 is being laid and fixed to the package 12.

[0100] Thus, when it is possible to prepare the both sides of the inferior surface of tongue of a chip (this example the 2nd chip 40) and a top face the pad which should be connected, it becomes easy to carry out the laminating of the chip of three or more layers. In this case, the 1st chip 8 corresponds to the 1st substrate, and the 2nd chip 40 corresponds to the 2nd substrate.

[0101] In addition, when connecting electrically through wiring (not shown) with which the 1st chip 8 and the 3rd chip 42 were formed in the 2nd chip 40 when the three or more layer laminating of the chip was carried out (for example, a case like drawing 10), the 3rd chip 42 also corresponds to the 2nd substrate. Moreover, when the 2nd chip 40 corresponds to the 1st substrate, the 1st chip 8 and the 3rd chip 42 correspond to the 2nd substrate.

[0102] In addition, in each above-mentioned operation gestalt, although FPGA was explained to the example as an example of the 1st programmable function part, this invention is not limited to this. For example, this invention can be applied also when PLA which is a kind of PLD as the 1st programmable function part is used.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the drawing in which the cross-section configuration of LSI (large scale integration)2 which is a semiconductor device by 1 operation gestalt of this invention is shown.

[Drawing 2] It is the decomposition perspective view of the laminating chip 4.

[Drawing 3] It is the drawing in which an example of the circuitry of the logic array 20 which constitutes FPGA formed in the 1st chip 8 was shown typically.

[Drawing 4] Drawing 4 A, drawing 4 B, and drawing 4 C are drawings in which the example of a programmable switching means is shown.

[Drawing 5] It is the drawing in which an example of the circuitry of the switch SW11 which used the memory using a ferroelectric is shown.

[Drawing 6] It is the drawing in which the cross-section configuration of the laminating chip by other operation gestalten of this invention is shown.

[Drawing 7] It is the drawing in which the cross-section configuration of the laminating chip by other operation gestalten of this invention is shown.

[Drawing 8] It is the drawing in which the cross-section configuration of the laminating chip by other operation gestalten of this invention is shown.

[Drawing 9] It is the drawing in which the cross-section configuration of the laminating chip by other operation gestalten of this invention is shown.

[Drawing 10] It is the drawing in which the cross-section configuration of the laminating chip by other operation gestalten of this invention is shown.

[Drawing 11] It is the decomposition perspective view of the laminating chip by other operation gestalten of this invention.

[Drawing 12] It is the functional block diagram showing the configuration of the compact disc system 60.

[Description of Notations]

2 ..... LSI

4 ..... Laminating chip

6 ..... The 2nd chip

6a, 6b .... Pad

8 ..... The 1st chip

8a, 8b .... Pad